

REMARKS

Claims 41-63 and 87-96 are withdrawn in this paper. Claims 1-8, 11, 13-31, 64-76 and 79-86 are now pending. Reconsideration of the above-referenced application in light of the amendments and following remarks is requested.

Claims 1-8, 11, 13-31, 64-76, 79-82 and 83-86 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by, or, in the alternative, under 35 U.S.C. § 103(a) as allegedly being obvious over Bright using common knowledge in the art or in view of Nakagawa, Juskey, Higgins III, Gore, or Tracy. Reconsideration is respectfully requested.

The Office Action contends that Bright teaches a “chip carrier 14 (socket); at least one integrated circuit chip 16 . . . a first magnetic field shielding material 18 (heat sink) . . . and a second magnetic field shielding material 12 in contact with said chip carrier.” (Office Action, pgs. 3-4). Applicant respectfully disagrees.

Bright merely teaches “an electrically-conductive frame 12 surrounding the edge of a socket 14 for receiving the electronic package 16.” (Col. 4, lines 50-53). Bright does not teach or suggest a chip carrier (allegedly element 14). Element 14 is a socket with dielectric housing 38 and openings 41 (Col. 5, lines 17-19). A conventional chip carrier is fabricated “from a substrate 20, an insulating layer 14, a plurality of conductive traces 15 (Figure 2) and an elastomeric layer 16.” (Applicant’s specification, pg. 1, lines 14-17). Bright’s socket does not have a substrate, an insulating layer, a plurality of conductive traces or even an elastomeric layer. Accordingly, Bright’s socket is not a chip carrier.

Bright does not teach or suggest an integrated circuit chip (allegedly element 16). Bright does not teach a first magnetic field shielding material (allegedly element 18). Element 18 is a heat sink which includes cooling towers 52 and four skirts extending downward outside the sidewalls 26, 30 of frame 12 (Col. 5, lines 30-66). “The engagement between skirts 56 [heat sink 18] and beams 32 grounds the sink 18 to the ground circuits (not shown) of substrate 72, and prevents it from acting as an antenna.”

(Col. 6, lines 2-5) (emphasis added). Stated in another manner, Bright's heat sink 18 is designed not to be conductive or have conductive properties since it is grounded to ground circuits of substrate 72. Accordingly, heat sink 18 is not a magnetic field shielding material nor does it act inherently as one.

Bright does not teach a second magnetic field shielding material (allegedly element 12). Element 12 is a frame that enables "grounding the heat sink when it is in place in the assembly of FIG. 1." (Col. 5, lines 1-2). Bright merely teaches "a novel assembly of socket and frame in which the frame is securely but releasably fastened to the socket, whereby the socket and frame can be handled, stored, packaged, sold and used as a unit, rather than providing two separate pieces." (Col. 6, lines 54-59).

To achieve this end, Bright provides a "frame . . . which has resilient locking tabs on its inner sides." (Col. 6, lines 60-61). Bright does not teach a structure with two magnetic field shielding materials. The heat-sink 18 is simply not a magnetic field shielding material. Even assuming arguendo that heat sink retainer 18 is a magnetic field shielding material, which it is not, Bright's heat sink retainer 18 is not in contact with electronic package 16, as recited in claim 1. "Heat sink 18 is placed over electronic package 16, with a thin thermal interface or blanket (not shown) placed therebetween." (Col. 5, lines 65-67) (emphasis added). Further, claims 1, 64 and 70, each recite a "magnetic random access memory device." Bright fails to teach or suggest the memory device of claims 1, 64 and 70.

Accordingly, Bright does not teach an integrated circuit structure comprising, "a chip carrier, at least one integrated circuit chip . . . being supported by a chip carrier . . . a first magnetic field shielding material in contact with said back surface of said chip, and a second magnetic field shielding material in contact with said chip carrier," as recited in claim 1 (emphasis added), "a die carrier, a die electrically connected to said die carrier, said die being in contact with a first layer of a magnetic field shielding material . . . a printed circuit board electrically connected to said die carrier . . . in contact with a second layer of

magnetic field shielding material,” as recited in claim 64 (emphasis added), or a method of packaging a semiconductor device comprising “electrically coupling a die carrier to a first surface of a die . . . contacting said second surface of said die with a first layer of magnetic field shielding material . . . contacting said die carrier with a second layer of magnetic field shielding material,” as recited in claim 70 (emphasis added).

The Office Action contends that Bright’s socket 14 “is a flip-chip carrier (since chip 16 is a flip-chip).” (Office Action, pg. 4). There is no support for this assertion. Bright does not teach or suggest that “said chip carrier is a flip-chip carrier,” as recited in claim 11. This is an additional reason for the allowance of claim 11. As described above, a conventional flip-chip carrier is one that comprises a substrate, an insulating layer, a plurality of conductive traces, and an elastomeric layer. Bright’s socket is not a flip-chip carrier.

The Office Action relies upon Nagakawa, Higgins or Gore to teach a printed circuit board with an additional layer of magnetic field shielding material. The Office Action concludes that although Bright “fails to teach that PCB 72 is in contact with an additional layer of magnetic field shielding material . . . the use of layers of magnetic field shielding material in an around PCB’s for the purpose of shielding EMI . . . is known in the art.” (Office Action, pg. 5) (emphasis added).

Applicant respectfully submits that this is improper hindsight reconstruction. There is simply no teaching or suggestion in any of the cited references to provide “a die carrier, a die electrically connected to said die carrier, said die being in contact with a first layer of a magnetic field shielding material . . . a printed circuit board electrically connected to said die carrier . . . in contact with a second layer of magnetic field shielding material,” as recited in claim 64 (emphasis added), or a “printed circuit board further comprises a third magnetic field shielding layer,” as recited in claim 20, or a “printed circuit board further comprises a fourth magnetic field shielding layer,” as recited in claim 27.

The cited references do not teach “wherein said die carrier comprises a third layer of magnetic field shielding material,” as recited in claim 65, or “a third layer of magnetic field shielding material is formed on surface of said printed circuit board,” as recited in claim 72.

The Office Action further asserts that , “[n]eedless to say, at the time the invention was made, PCB having multiple metal layers and multiple-layered ground paths in different layers, including top, bottom, and embedded, is known in the art.” (Office Action, pg. 6). However, the Office Action has not provided support for this assertion. The prior art does not teach or suggest forming a third or fourth layer of magnetic field shielding material. Much less, in conjunction with a chip carrier comprising a semiconductor chip having a first and second layer of magnetic field shielding material.

The cited references do not teach or suggest, a “third layer of magnetic field shielding material is formed on a top surface of said printed circuit board,” as recited in claim 73, a “third layer of magnetic field shielding material is formed on a bottom surface of said printed circuit board,” as recited in claim 74, a “third layer of magnetic field shielding material is embedded within said printed circuit board,” as recited in claim 75, a “third magnetic field shielding layer [which] is located on said upper surface of said printed circuit board,” as recited in claim 21, a “third magnetic field shielding layer [which] is located on said bottom surface of said printed circuit board,” as recited in claim 22, or a “third magnetic field shielding layer [which] is embedded within said printed circuit board,” as recited in claim 23.

For at least these reasons, independent claims 1, 64 and 70 are allowable over the cited references. Claim 2-8, 11 and 13-31 depend from claim 1 and should be allowable for at least the same reasons as for allowance of independent claim 1. Claim 65-69 depend from claim 64 and should be allowable for at least the same reasons as for allowance of independent claim 64. Claim 71-76, 83-86 and 79-82 depend from claim 70 and should be allowable for at least the same reasons as for allowance of independent claim 70.

Claims 1-8, 11, 13-31, 64-76, 83-86 and 79-82 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by, or, in the alternative, under 35 U.S.C. § 103(a) as allegedly being obvious over Mertol using common knowledge in the art or in view of Nakagawa, Juskey, Higgins III, Gore, or Tracy. Reconsideration is respectfully requested.

The Office Action alleges that Mertol teaches “a chip carrier 22/36, at least one integrated circuit chip 10 . . . a first magnetic field shielding material 26 (heat spreader) in contact with said back surface of said chip, and a second magnetic field shielding material 30 in contact with said chip carrier.” (Office Action, pg. 8). Applicant respectfully disagrees.

Mertol merely teaches that “the use of grounding leads 16 to connect the electrically conductive stiffener 24 and heat spreader 26 to an electrical ground potential forms an electromagnetic shield around semiconductor device 20.” (Col. 10, lines 28-32) (emphasis added). The use of grounding leads 16 creates the electromagnetic shield and not through the presence of heat spreader 26 by itself.

Mertol does not teach or suggest a chip carrier (allegedly element 36). Element 36 is an adhesive layer and element 22 is the substrate (Col. 8, lines 58-60). Mertol does not teach a first magnetic field shielding material (allegedly element 26). Element 26 is a heat spreader which “efficiently conducts heat energy from chip 10 either to a heat sink attached to a substantially planar upper surface of heat spread 26 or . . . to an ambient surrounding semiconductor device 20.” (Col. 9, lines 50-54) (emphasis added). As described previously, the presence of heat spreader 26 by itself does not provide an electromagnetic shield.

Mertol does not teach a second magnetic field shielding material (allegedly element 30). Element 30 is a horizontal trace conductor that electrically connects bond pad 32 to bond pad 34 (Col. 8, lines 40-44). Mertol merely teaches an electromagnetic shield formed around the semiconductor device 20. Mertol does not teach or suggest

multiple magnetic field shielding material layers as recited in claims 1, 64 and 70.

Moreover, Mertol teaches that “a layer of thermal interface material 40 is formed upon the upper surface of chip 10, and an underside surface of heat spreader 26 is attached to an upper surface of substrate 22.” (Col. 9, lines 55-58) (emphasis added). As a result, “the thermal interface material spreads out between the upper surface of chip 10 and the adjacent portion of the underside of heat spreader 26 to form thermal interface layer 40 therebetween.” (Col. 10, lines 5-8) (emphasis added). Even assuming arguendo that heat spreader 26 is magnetic field shielding material, which it is not, Mertol’s heat spread 26 is not in direct contact with the semiconductor chip, as recited in claims 1, 64 and 70.

Accordingly, Mertol does not teach an integrated circuit structure comprising, “a chip carrier, at least one integrated circuit chip . . . being supported by a chip carrier . . . a first magnetic field shielding material in contact with said back surface of said chip, and a second magnetic field shielding material in contact with said chip carrier,” as recited in claim 1 (emphasis added), “a die carrier, a die electrically connected to said die carrier, said die being in contact with a first layer of a magnetic field shielding material . . . a printed circuit board electrically connected to said die carrier . . . in contact with a second layer of magnetic field shielding material,” as recited in claim 64 (emphasis added), or a method of packaging a semiconductor device comprising “electrically coupling a die carrier to a first surface of a die . . . contacting said second surface of said die with a first layer of magnetic field shielding material . . . contacting said die carrier with a second layer of magnetic field shielding material,” as recited in claim 70 (emphasis added).

The Office Action relies upon Nagakawa, Higgins or Gore to teach a printed circuit board with an additional layer of magnetic field shielding material. The Office Action concludes that although Mertol “fails to explicitly disclose a PCB and fails to disclose that the PCB is in contact with an additional layer of magnetic field shielding material . . . the use of layers of magnetic field shielding material in and around PCB’s for the purpose of shielding EMI . . . is known in the art.” (Office Action, pg. 9) (emphasis

added).

Applicant respectfully submits that this is improper hindsight reconstruction. There is simply no teaching or suggestion in any of the cited references to provide “a die carrier, a die electrically connected to said die carrier, said die being in contact with a first layer of a magnetic field shielding material . . . a printed circuit board electrically connected to said die carrier . . . in contact with a second layer of magnetic field shielding material,” as recited in claim 64 (emphasis added), or a “printed circuit board further comprises a third magnetic field shielding layer,” as recited in claim 20, or a “printed circuit board further comprises a fourth magnetic field shielding layer,” as recited in claim 27.

The cited references do not teach “wherein said die carrier comprises a third layer of magnetic field shielding material,” as recited in claim 65, or “a third layer of magnetic field shielding material is formed on surface of said printed circuit board,” as recited in claim 72.

The Office Action further asserts that ,”[n]eedless to say, at the time the invention was made, PCB having multiple metal layers and multiple-layered ground paths in different layers, including top, bottom, and embedded, is known in the art.” (Office Action, pg. 6). However, the Office Action has not provided any support for this assertion. The prior art does not teach or suggest forming a third or fourth layer of magnetic field shielding material. Much less, in conjunction with a chip carrier comprising a semiconductor chip having a first and second layer of magnetic field shielding material.

The cited references do not teach or suggest, a “third layer of magnetic field shielding material is formed on a top surface of said printed circuit board,” as recited in claim 73, a “third layer of magnetic field shielding material is formed on a bottom surface of said printed circuit board,” as recited in claim 74, a “third layer of magnetic field shielding material is embedded within said printed circuit board,” as recited in claim 75, a “third magnetic field shielding layer [which] is located on said upper surface of said printed circuit board,” as recited in claim 21, a “third magnetic field shielding layer [which] is

located on said bottom surface of said printed circuit board,” as recited in claim 22, or a “third magnetic field shielding layer [which] is embedded within said printed circuit board,” as recited in claim 23.

For at least these reasons, independent claims 1, 64 and 70 are allowable over the cited references. Claim 2-8, 11 and 13-31 depend from claim 1 and should be allowable for at least the same reasons as for allowance of independent claim 1. Claim 65-69 depend from claim 64 and should be allowable for at least the same reasons as for allowance of independent claim 64. Claim 71-76, 83-86 and 79-82 depend from claim 70 and should be allowable for at least the same reasons as for allowance of independent claim 70.

Claims 1-8, 11, 13-31, 64-76, 83-86 and 79-82 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by, or, in the alternative, under 35 U.S.C. § 103(a) as allegedly being obvious over Bright using common knowledge in the art or in view of Nakagawa, Juskey, Higgins III, Gore, or Tracy. Reconsideration is respectfully requested.

For at least the reasons provided above, the cited references do not teach or suggest Applicant’s claimed invention. In particular, Bright does not teach an integrated circuit structure comprising, “a chip carrier, at least one integrated circuit chip . . . being supported by a chip carrier . . . a first magnetic field shielding material in contact with said back surface of said chip, and a second magnetic field shielding material in contact with said chip carrier,” as recited in claim 1 (emphasis added), “a die carrier, a die electrically connected to said die carrier, said die being in contact with a first layer of a magnetic field shielding material . . . a printed circuit board electrically connected to said die carrier . . . in contact with a second layer of magnetic field shielding material,” as recited in claim 64 (emphasis added), or a method of packaging a semiconductor device comprising “electrically coupling a die carrier to a first surface of a die . . . contacting said second surface of said die with a first layer of magnetic field shielding material . . . contacting said die carrier with a second layer of magnetic field shielding material,” as recited in claim 70 (emphasis added).

Application No.: 09/653,541

Docket No.: M4065.0363/P363

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: August 11, 2003

Respectfully submitted,

By 

Thomas J. D'Amicp

Registration No.: 28,371

DICKSTEIN SHAPIRO MORIN &

OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 828-2232

Attorney for Applicant